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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,946	12/20/2000	Steven W. Rogers	5150-52100	8700

35690 7590 01/08/2008

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
KE, PENG	

ART UNIT	PAPER NUMBER
2174	

MAIL DATE	DELIVERY MODE
01/08/2008	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/742,946
Filing Date: December 20, 2000
Appellant(s): ROGERS ET AL.

Rogers and King
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/22/07 appealing from the Office action mailed 4/7/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 6,117,183	**Teranishi**	**9-2000**
US 5,481,741	**McKaskle**	**1-1996**

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections – 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14, 16-29, and 31-52 are rejected under 35 U.S.C. 102(e) as being anticipated by Teranishi et al. U.S. Patent 6,117,183.

As per claim 1, Teranishi e al teaches a method for propagating type information for hardware device nodes in a graphical program, wherein the method operates in a computer including a display screen and a user input device, the method comprising:

displaying on the display screen of the computer a first hardware device node in the graphical program in response to user input, wherein the graphical program comprises a plurality of interconnected nodes or icons, wherein the plurality of interconnected nodes or icons visually indicate functionality of the graphical program; (see Teranishi, column 7, lines 40-55)

associating the first hardware device node with a hardware device; (see Teranishi, column 7, lines 40-55)

displaying on the display screen a second hardware device node in the graphical program in response to user input; (see Teranishi, column 7, lines 40-55)

connecting the first hardware device node to the second hardware device node in response to user input; (see Teranishi, column 7, lines 40-55)

propagating information from the first hardware device node to the second hardware device node, wherein the information specifies the hardware device with which the first hardware device node is associated, wherein said propagating occurs in response to said connecting the first hardware device node to the second hardware device node; (see Teranishi, column 4, lines 5-26)

wherein the graphical program is executable by the computer. (see Teranishi, column 12, lines 20-41)

As per claim 2, which is dependent on claim 1, Teranishi teaches the method of claim 1. Teranishi further teaches wherein said displaying the first and second hardware device nodes in the graphical program comprises including the first and second hardware device nodes in a block diagram of the graphical program, wherein the block diagram visually indicates functionality of the graphical program. (see Teranishi, Figure 7, items L01-L04)

As per claim 3, which is dependent on claim 1, Teranishi teaches the method of claim 1. Teranisi further teaches comprising: associating the second hardware device node with the hardware device with which the first hardware device node is associated, in response to said propagating the information to the second hardware device node. (see Teranishi, column 4, lines 5-26)

As per claim 4, which is dependent on claim 1, Teranishi teaches the method of claim 1. Teranishi further teaches wherein said connecting the first hardware device node to the second hardware device node comprises connecting a wire from an output terminal of the first hardware device node to an input terminal of the second hardware device node. (see Teranishi, Figure 7, items L01-L04, column 7, lines 40-55; It is inherent that there must be an input terminal and an output terminal for the connection between L02 and L01)

As per claim 5, which is dependent on claim 1, Teranishi teaches the method of claim 1. Terranishi further teaches the method wherein said associating the first hardware device node with a hardware device comprises associating the first hardware device node with a hardware device class corresponding to the hardware device; wherein said propagating information from the first hardware device node to the second hardware device node comprises propagating information specifying the hardware device class with which the first hardware device node is associated. (see Teranishi, column 4, lines 5-26)

As per claim 6, which is dependent on claim 1. Teranishi teaches the method of claim 5. Terranishi further teaches the method comprising: associating the second hardware device node with the hardware device class, in response to said propagating the information to the second hardware device node. (see Teranishi, column 4, lines 5-26)

As per claim 7, which is dependent on claim 6. Teranishi teaches the method of claim 6. Terranishi further teaches the method comprising: associating the second hardware device node with a method of the hardware device class in response to user input; wherein during execution of the graphical program the second hardware device node is operable to invoke the method. (see Teranishi, column 4, lines 5-26, column 12, lines 20-41)

As per claim 8, which is dependent on claim 6, Terranishi teaches the method of claim 6. Terranishi further teaches the method comprising: associating the second hardware device node with a property of the hardware device class in response to user input; wherein during execution of the graphical program the second hardware device node is operable to perform one or more of: 1) getting the property; and 2) setting the property.(see Terranishi, column 4, lines 4-58)

As per claim 9, which is dependent on claim 1, Terranishi teaches the method of claim 1. Terranishi further teaches the method comprising: executing the graphical program, wherein during execution of the graphical program the second hardware device node is operable to access the hardware device. (see Terranishi, column 4, lines 58-column 5,lines 23)

As per claim 10, Teranshi teaches a method for performing type checking for a hardware device node in a graphical program, wherein the method operates in a computer including a display screen, the method comprising:

displaying on the display screen of the computer a first hardware device node in the graphical program in response to user input, wherein the graphical program comprises a plurality

of interconnected nodes or icons, wherein the plurality of interconnected nodes or icons visually indicate functionality of the graphical program; (see Teranishi, column 7, lines 40-55)

associating the first hardware device node with a first hardware device class in response to user input; (see Teranishi, column 7, lines 40-55)

selecting a method or property of the first hardware device class for the first hardware device node in response to user input; (see Teranishi, column 7, lines 40-55)

changing the first hardware device node to have an association with a second hardware device class in response to user input; (see Teranishi, column 4, lines 27-55)

and

performing type checking to determine whether the method or property is valid for the second hardware device class, in response to said changing the first hardware device node to have an association with the second hardware device class; (see Teranishi, column 5, lines 6-23)

wherein the graphical, program is executable by the computer. (see Teranishi, column 12, lines 20-41)

As per claim 11, which is dependent on claim 10. Teranshi teaches the method of claim 10. Teranshi further teaches the method comprising: indicating an invalid condition if the method or property is not valid for the second hardware device class. (see Teranshi, column 6, lines 58-column 7, lines 10)

As per claim 12, which is dependent on claim 11. Teranshi teaches the method of claim 11. Teranshi further teaches the method wherein said indicating the invalid condition comprises altering the visual appearance of a wire connected to an input terminal of the first hardware device node, wherein the wire provides information specifying the second hardware device class with which the first hardware device node is associated. (see Teranshi, column 6, lines 58-column 7, lines 10)

As per claim 13, which is dependent on claim 11. Teranshi teaches the method of claim 10. Teranshi further teaches method comprising:

preventing execution of the graphical program if the method or property is not valid for the second hardware device class. (see Teranshi, column 8, lines 30-35)

As per claim 14, which is dependent on claim 11. Teranshi teaches the method of claim 10. Teranshi further teaches the method wherein the first hardware device node has an input terminal for receiving information specifying a hardware device class with which to associate the first hardware device node; (see Teranishi, column 4, lines 27-55)

wherein said associating the first hardware device node with the first hardware device class comprises connecting a first wire to the input terminal; (see Teranishi, column 4, lines 27-55)

wherein said changing the first hardware device node to have an association with a second hardware device class comprises connecting a second wire to the input terminal. (see Teranishi, column 4, lines 27-55)

As per claim 16, which is dependent on claim 10. Teranshi teaches the method of claim 10. Teranshi further teaches the method wherein said performing type checking to determine whether the method or property is valid for the second hardware device class comprises: determining a list of valid methods and properties for the second hardware device class; and

determining whether the method or property is included in the list of valid method and properties. (see Teranshi, column 6, lines 58-column 7, lines 10)

As per claim 17, which is dependent on claim 16. Teranshi teaches the method of claim 16. Teranshi further teaches the method wherein said determining the list of valid methods and properties for the second hardware device class comprises determining the valid methods and

properties from a type library, wherein the type library includes information regarding the second hardware device class. (see Teranshi, column 7, lines 26-40)

As per claim 18, it is rejected with same rationale as claim 1. (see rejection above)

As per claim 19, which is dependent on claim 18, it is of the same scope as claim 2. (see rejection above)

As per claim 20, which is dependent on claim 18, it is of the same scope as claim 3. (see rejection above)

As per claim 21, which is dependent on claim 18, it is of the same scope as claim 4. (see rejection above)

As per claim 22, which is dependent on claim 18, it is of the same scope as claim 5. (see rejection above)

As per claim 23, which is dependent on claim 22, it is of the same scope as claim 6. (see rejection above)

As per claim 24, which is dependent on clam 23, it is of the same scope as claim 7. (see rejection above)

As per claim 25, which is dependent on claim 23, it is of the same scope as claim 8. (see rejection above)

As per claim 26, it is rejected with the same rationale as claim 10. (see rejection above)

As per claim 27, which is dependent on claim 26, it is of the same scope as claim 11. (see rejection above)

As per claim 28, which is dependent on claim 26, it is of the same scope as claim 13. (see rejection above)

As per claim 29, which is dependent on claim 26, it is of the same scope as claim 14. (see rejection above)

As per claim 31, which is dependent on claim 26, it is of the same scope as claim 16. (see rejection above)

As per claim 32, it is rejected with same rationale as claim 1. (see rejection above)

As per claim 33, which is dependent on claim 32, it is of the same scope as claim 2. (see rejection above)

As per claim 34, which is dependent on claim 32, it is of the same scope as claim 3. (see rejection above)

As per claim 35, which is dependent on claim 32, it is of the same scope as claim 5. (see rejection above)

As per claim 36, which is dependent on claim 35. Teranshi teaches the system of claim 35. Teranshi further teaches the system processor is further operable to execute program instructions stored in the memory to associate the second hardware device node with the hardware device class, in response to said propagating the information to the second hardware device node. (see Teranishi, column 4, lines 27-55)

As per claim 37, which is dependent on claim 36, it is of the same scope as claim 7. (see rejection above)

As per claim 38, which is dependent on claim 36, it is of the same scope as claim 8. (see rejection above)

As per claim 39, it is rejected with same rationale as claim 10. (see rejection above)

As per claim 40, which is dependent on claim 39, it is of the same scope as claim 16. (see rejection above)

As per claim 41, which is dependent on claim 39, Teranishi teaches the claim 39. Teranishi further teaches the graphical program is interpretable or compliable to generate instructions executable by the computer. (see Teranishi, column 12, lines 20-41)

As per claim 42, which is dependent on claim 39, Teranishi teaches the claim 39. Teranishi further teaches the graphical program comprises a dataflow diagram. (figure 3, items a-c)

As per claim 43, which is dependent on claim 32, it is of the same scope as claim 41. (see rejection above)

As per claim 44, which is dependent on claim 32, it is of the same scope as claim 42. (see rejection above)

As per claim 45, which is dependent on claim 26, it is of the same scope as claim 41. (see rejection above)

As per claim 46, which is dependent on claim 26, it is of the same scope as claim 42. (see rejection above)

As per claim 47, which is dependent on claim 18, it is of the same scope as claim 41. (see rejection above)

As per claim 48, which is dependent on claim 18, it is of the same scope as claim 42. (see rejection above)

As per claim 49, which is dependent on claim 10, it is of the same scope as claim 41. (see rejection above)

As per claim 50, which is dependent on claim 10, it is of the same scope as claim 42. (see rejection above)

As per claim 51, which is dependent on claim 1, it is of the same scope as claim 41. (see rejection above)

As per claim 52, which is dependent on claim 1, it is of the same scope as claim 42. (see rejection above)

Claim Rejections – 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Teranishi et al. U.S. Patent 6,117,183 further in view of McKaskle et al. US Patent 5,481,741.

As per claim 15, Teranishi teaches the method of claim 10. However he fails to teach the method wherein the first hardware device node is a register access node.

McKaskle et al. teaches a wherein the first hardware device node is a register access node. (figure 100 a-d)

It would have been obvious to an artisan at the time of the invention to include McKaskle's teaching with method of Teranishi in order to allow users to simulate a control register.

As per claim 30, which is dependent on claim 26, it is of the same scope as claim 15. (see rejection above)

(10) Response to Argument

Claims 1, 18, and 32

Appellant's argument focused on the following issues:

A) Is Teranishi's CAD system a graphical program?

A) Teranishi's CAD system is a graphical program. (see Teranishi col. 7, lines 45-60) Although Appellants have suggested that a graphical program should be able to use a computer to interpret the diagram constructed by a user, Teranishi's CAD performs this function. (see Teranishi col. 8, lines 1-30) Teranishi's CAD system would use the CPU (see Teranishi col. 7, lines 45-60) to calculate the delayed time of the diagram designed by the user. (see Teranishi col. 8, lines 1-30)

B) Has Teranishi suggested propagating information from a first hardware device node to a second hardware device node of a graphical program?

B) During patent examination, the pending claims must be "given >their< broadest reasonable interpretation consistent with the specification." > In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be

interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

In this case, Teranishi teaches propagating information from a first hardware device node to a second hardware device node of a graphical program because Teranishi's CAD program passes position data of first hardware device node to the second hardware device in order to calculate the delay time between the two device node. (see Teranishi col. 8, lines 10-55)

C) Has Teranishi suggested presenting a node in graphical program as a representation of a hardware device?

C) Teranishi's node in graphical program is a representation of a hardware device. (see Teranishi, col. 7, lines 5-25) Teranishi's CAD, as described in its abstract, is an "apparatus for logic circuit packaging design, wherein provisions are made to display delay times in real time when a component is being moved…" (see, Teranishi's abstract) In Teranishi's CAD, each graphical node in the user's design diagram is a representation of a hardware component. (see Teranishi, col. 7, lines 5-25)

Claims 3, 20, and 24

Appellant's argument focused on the following:

A) Has Teranishi taught "associating the second hard ware device node with the hardware device with which the first hardware device node is associated, in response to said propagating the information to the second hardware device node" ?

A) Teranishi teaches "associating the second hard ware device node with the hardware device with which the first hardware device node is associated, in response to said propagating the information to the second hardware device node." (see Teranishi col. 8, lines 10-55)

Teranishi's CAD program passes position data of first hardware device node to the second hardware device in order to calculate the delay time between the two device node. (see Teranishi col. 8, lines 10-55) Then by associating the second hardware device node's position data with that of the first hardware device node, Teranishi is able to calculate the delay time and error rate between the two hardware device nodes. (see Teranishi col. 8, lines 10-55)

Claims 10, 26 and 39

Appellant's argument focused on the following:

A) Has Teranishi associate hardware device node with different component type and component class?

A) Teranishi did associate different hardware device node with different component type because different hardware device node is associated with different component property, which include different error levels and different line thickness or line type. (see Teranishi col. 6, lines 30-60, col. 7, lines 1-25)

Claims 16, 31, and 40

Appellant's argument focused on the following:

A) Has Teranishi associate hardware device node with different component type and component class?

A) Teranishi did associate different hardware device node with different component type because different hardware device node is associated with different component property, which include different error levels and different line thickness or line type. (see Teranishi col. 6, lines 30-60, col. 7, lines 1-25)

Claim 15 and 30.

Appellant's argument focused on the following:

A) Has McKaskle taught where the first hard ware device node is a register access node?

A) McKaskle teaches a class of register access node because it provides user with access to a shift register class nodes. (see McKaskle figure 100A-D, col. 49, lines 60-67)

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Peng Ke/

Examiner, Art Unit 2174

Conferees:

/SY D. LUU/

Primary Examiner, Art Unit 2174

/David A Wiley/

Supervisory Patent Examiner, Art Unit 2174